

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	734	configurat\$4 same bitstream	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:24
L2	267	L1 and code and instruct\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L3	152	L2 and transform\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L4	73	L2 and pld	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L5	17	L4 and segment	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L6	73	L2 and pld	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L7	30	L4 and arrange\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L8	31481	code same segment	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L9	80	L1 and L8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19

L10	63	L9 and instruct\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L11	2	L1 same L8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:19
L13	67	(configurat\$4 same bitstream same code) and instruct\$4 and arrang\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:36
L14	12	(configurat\$4 same bitstream same code) and instruct\$4 and arrang\$5 and transform\$4 and engine	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:36
L15	41	(configurat\$4 same bitstream same code) and instruct\$4 and arrang\$5 and transform\$4 and segment and function	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/21 19:39

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040190092 A1	20040930	244	Scanning device for coded data	358/539
2	US 20030144828 A1	20030731	237	Hub array system and method	703/21
3	US 20020152060 A1	20021017	207	Inter-chip communication system	703/17
4	US 6810442 B1	20041026	214	Memory mapping system and method	710/22
5	US 6785873 B1	20040831	191	Emulation system with multiple asynchronous clocks	716/4
6	US 6754763 B2	20040622	225	Multi-board connection system for use in electronic design automation	710/317
7	US 6651225 B1	20031118	179	Dynamic evaluation logic system and method	716/4
8	US 6421251 B1	20020716	134	Array board interconnect system and method	361/788
9	US 6389379 B1	20020514	157	Converification system and method	703/14
10	US 6321366 B1	20011120	165	Timing-insensitive glitch-free logic system and method	716/6
11	US 6134516 A	20001017	132	Simulation server system and method	703/27
12	US 6026230 A	20000215	131	Memory simulation system and method	703/13